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# ADC Offset

R[71205d037008]+

R[71205d037008]+R[71205d037008]+R[71205d037008]+

Table . Board #8

|  |  |  |  |
| --- | --- | --- | --- |
| Channel # | Bit 2 | Bit 1 | Bit 0 |
| 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 2 | 0 | 0 | 1 |
| 3 | 0 | 0 | 1 |

PER = 1 in 5003

BER = 1 in 201

Table 2. Board #10

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Channel # | Bit 2 | Bit 1 | Bit 0 | Frequency |
| 0 | 0 | 0 | 0 |  |
| 1 | 0 | 0 | 0 |  |
| 2 | 0 | 0  1  1 | 1  0  1 | 45%  45%  10% |
| 3 | 0 | 0 | 0 |  |

PER = 1 in 531

BER = 1 in 225

Table 3. Board #5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Channel # | Bit 2 | Bit 1 | Bit 0 | Frequency |
| 0 | 0 | 0 | 0 |  |
| 1 | 0 | 0 | 0 |  |
| 2 | 0 | 0 | 0 |  |
| 3 | 0 | 0 | 0 |  |

Not working

Table 4. Board #3

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Channel # | Bit 2 | Bit 1 | Bit 0 | Frequency |
| 0 | 0 | 1 | 0 |  |
| 1 | 0 | 1 | 0 |  |
| 2 | 0 | 1 | 0 |  |
| 3 | 0 | 1 | 0 |  |

Not working

Table 5. Board #2

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Channel # | Bit 2 | Bit 1 | Bit 0 | Frequency |
| 0 | 0 | 0 | 1 |  |
| 1 | 0 | 0  1 | 1  0 | 50%  50% |
| 2 | 0 | 0 | 0 |  |
| 3 | 0 | 0 | 0  1 | 25%  75% |

PER = 1 in 15000+

BER = 1 in 62

Table 6. Board #1

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Channel # | Bit 2 | Bit 1 | Bit 0 | Frequency |
| 0 | 0 | 0 | 0 |  |
| 1 | 0 | 0 | 1  0 | 50%  50% |
| 2 | 0  1 | 1  0 | 1  0 | 50%  50% |
| 3 | 0 | 0 | 0 |  |

PER = 1 in 15000+

BER = 1 in 133

Table 7. Board #7

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Channel # | Bit 2 | Bit 1 | Bit 0 | Frequency |
| 0 | 0 | 0 | 0 |  |
| 1 | 0 | 0 | 0 |  |
| 2 | 0 | 0 | 0 |  |
| 3 | 0 | 0 | 0 |  |

PER = 1 in 272

BER = 1 in 20

Table 8. Board #6

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Channel # | Bit 2 | Bit 1 | Bit 0 | Frequency |
| 0 | 0 | 0 | 0 |  |
| 1 | 0 | 0 | 0 |  |
| 2 | 0 | 0 | 0  1 | 95%  5% |
| 3 | 0 | 0 | 0 |  |

PER = 1 in 20

BER = 1 in 30